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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
550-546

Application Number	Filed
10/815,982	April 2, 2004
First Named Inventor: TRAN	
Art Unit: 7258	Examiner: Iwashko, Lev

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____

Signature

John R. Lastova
Typed or printed name

703-816-4025
Requester's telephone number

November 28, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Patent Application of

TRAN et al

Atty. Ref.: 550-546; Confirmation No. 2186

Appl. No. 10/815,982

TC/A.U. 7258

Filed: April 2, 2004

Examiner: Iwashko, Lev

For: DATA TRANSFER BETWEEN AN EXTERNAL DATA SOURCE AND A MEMORY ASSOCIATED WITH A DATA PROCESSOR

* * * * * * * * * * *

November 28, 2006

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Commissioner for Patents
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Sir:

PRE-APPEAL BRIEF

This pre-appeal brief is in response to the final Official Action dated August 30, 2006. The primary rejection is that of claims 1-8, 10-15, 17-20, 22, 24,-31, and 33-36 under 35 U.S.C. 102(e) for anticipation by US patent publication 2003/0135699 A1 to Matsuzaki. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Matsuzaki fails to satisfy this rigorous standard.

Matsuzaki relates to a semiconductor memory device rather than to a data processor core. It discloses a multi-port memory device with multiple ports that allow independent access to the memory from the different ports. Matsuzaki addresses the problem of a DRAM memory not allowing access from one port to a given block if another port is already accessing that block. An internal circuit provides external commands from the ports to an arbitration circuit which generates an enable signal that allows a port signal port to be transmitted to the core. The core is clocked by the clock signal associated with the port in response to the enable signal.

The application describes a processor core (e.g., 10 in Figure 1) that is divided into portions including a data processing portion (e.g., 12 in Figure 1) and a memory access portion (e.g., 30 in Figure 1). The portions are independently (e.g., HCLKEN(1) and (2) in Figure 1) enabled to allow data to be transferred via the memory access interface when the processor core is sleeping. Moreover, the core can operate when the memory access interface is not operating.

Because Matsuzaki relates to a different technical field and is not concerned with the same problem as are the claims in this case relating to transferring data via the processor core from a slower memory (e.g., FLASH memory) to a faster memory (e.g., instruction memory), it is not surprising that multiple claim features are not disclosed in Matsuzaki. Each missing feature from independent claims 1 and 25 is a "clear error" in the Examiner's anticipation rejection. Just one missing feature requires that the rejection be withdrawn.

First, Matsuzaki fails to disclose "a data processor core" as recited all independent claims. The Examiner does not identify a particular element in Matsuzaki or any section of text in Matsuzaki where a data processor core is disclosed. A DRAM core is a memory and not a data processor core. The Examiner wrongly dismisses this deficiency arguing that the distinction can

be ignored because the data processor core "is referenced in the preamble, which does not give it any weight of patentability." This statement is wrong with respect to the law and the facts.

Regarding the law, the Federal Circuit has found in many instances that features in preambles are to be given weight as a matter of law. For example, terminology in the preamble that limits the structure of the claims must be treated as a claim limitation. See e.g., *Pac-Tec Inc. v. Amerace Corp.*, 903 F.2d 796, 801 (Fed. Cir. 1990). Moreover, a "claim preamble has the import that the claim as a whole suggests for it." *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995). Still further, "[i]f the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim." *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298 (Fed. Cir. 1999).

In this case, one need not even perform the various preamble analyses required in the *Pac-Tec*, *Bell Communications*, and *Pitney Bowes* cases because the term "data processor core" defined in the preamble is explicitly referred to and used in the body of claim 1. For example, claim 1 explicitly incorporates the claimed "data processor core" recited in the preamble into the body of the claim by twice referring to "said data processor core" in lines 6 and 12. Moreover, a data processor core recites structure—it is not simply a field of use or an intended use. To ignore the fact that independent claims 1 and 25 are directed to a data processor core requires—contrary to well-established law—that the claim body be read out of context, and without the context of a data processor core, claims 1 and 25 lack meaning. Accordingly, the Examiner's reading is a clear error.

The claims are clearly directed to a different device than that described by Matsuzaki. No one skilled in the data processing arts would reasonably suggest that a semiconductor memory is a data processor core. Because Matsuzaki lacks a data processor core as required by the claims, the anticipation rejection is in error and must be withdrawn.

Second, Matsuzaki does not disclose "a data processing portion operable to perform further data processing operations." The Examiner relies on section 0141 lines 1-4 and Figure 121. But these operations are not data processing operations performed by a data processing portion. Rather, those operations are performed by a memory core, which in this particular example, relate to inputting and outputting data via input/output ports. The Examiner dismisses this distinction again based on the erroneous contention that claiming a data processing core "is irrelevant." But how can the very thing that the claims recite be irrelevant in a prior art analysis?

Third, Matsuzaki fails to teach a data processing portion enabled by a data processing enable signal and the memory access interface portion enabled by a memory access enable signal, and otherwise, the different portions do not receive the processor clock signal. Initially, the Examiner contended that Figure 1 "demonstrates" this limitation. But Figure 1 merely shows the timing of demands received at ports A and B which are the external ports of a semiconductor memory device. The Figure shows how the read and write commands are completed within clock cycles. There is no disclosure of a data processing portion or a data processing enable signal, let alone the reception by the data processing portion of clock signals only when the enable signal has a certain value.

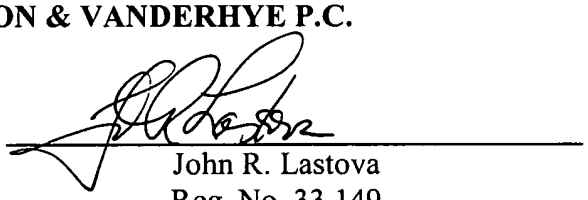
In response to Applicants' arguments, the Examiner now refers to the clock signal CLKA and section 0579 in Matsuzaki. The memory core in Matsuzaki only allows a single port to access the memory at any one time by using enable signals that allow the memory to be clocked

by the port clock. See for example the reference to Figure 119 in section 13 of the final action. Thus, *each* port can enable *one* memory core by sending a clock signal to it. There is no disclosure of *two different portions* of the memory core receiving clock signals in response to separate enable signals corresponding to these different portions. But this is besides the main point that Matsuzaki fails to disclose the claimed separate enablement of a data processing portion and a memory access interface portion. The only enablement described in Matsuzaki is in memory.

The application is in condition for allowance. An early notice to that effect is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
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